KANDOU BUS

KANDOU'S INTERFACES FOR HIGH SPEED SERIAL LINKS

WHITE PAPER

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Summary

Kandou Bus has developed an important new approach to serial link design that increases the bit rate for a given physical communications bus. With this technology more bits can be sent per unit of energy, or less energy can be used to achieve a given bit rate. For many common high-speed links, the link can be improved by some combination of a speed increase of a factor of 1.5 to 4 and/or a total link power consumption reduction of a factor of 2-4. These gains are complementary (thus additive) to known advanced link design techniques in use today. The magnitude and potential for tradeoffs of these gains dramatically improves the constraint space across numerous aspects of the design of high-speed electronic devices.

Introduction

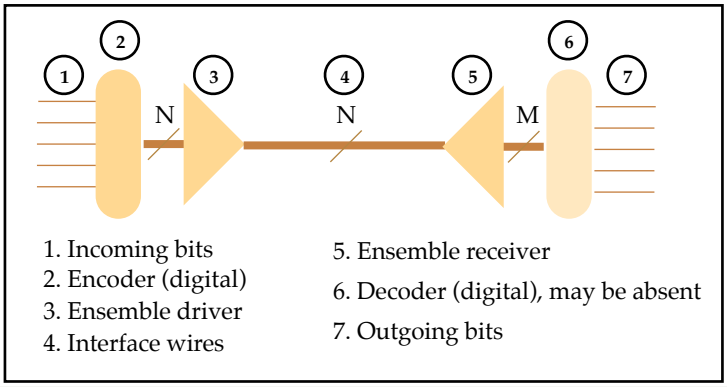
In today's world, almost all electronic devices are enhanced by having ever faster communications capabilities. As a result, designers are striving to make the overall component and system communication faster and faster. The speed of a communication link, the energy it uses, and its physical footprint are of primary interest to designers of such electronic devices. The energy in particular is a scarce resource that is often depleted too rapidly. Unfortunately, the pursuit of speed exacerbates the problem as it is often achieved by increasing energy consumption of key components such as the communication bus.

Energy used by communication between components varies widely by the function and the design of the underlying system. In order to satisfy the increasing demand for data transfer between IC components, it is therefore imperative to create techniques for lowering the energy consumption at a given communication speed and a given signal integrity. This not only drives lower energy consumption at today's speeds, but also makes possible much greater overall communication speeds.

Many different engineering approaches to lowering energy consumption and increasing bit rates are in use by the research and industrial community. These techniques include lowering the voltage swing and Vdd to lower energy consumption, adding passive shielding to mitigate crosstalk and allow for higher transmission speeds, and designing smart architectures with power-down modes to minimize energy consumption. Kandou Bus offers a completely new approach to this problem, called Chord™ signaling, that is complementary to these engineering approaches. This approach solves the problem by changing the basic signaling on the communication wires. As compared to the ubiquitous differential NRZ (Non-Return to Zero) signaling, Kandou's Chord™ signaling techniques lead to the transfer of more bits per wire using less power. As compared to traditional single-ended signaling, Chord™ signaling offers higher signal integrity, which can be translated to either less power used for every bit delivered, or a larger number of bits delivered for a given power consumption. As compared to other advanced signaling methods, for example multi-level signaling methods such as PAM-4, Chord™ signaling provides much better immunity to Inter-Symbol Interference (ISI) and other types of noise, and allows for the use of simpler equalization techniques that are implementable with a lower power consumption and with a smaller footprint for a given channel and throughput. These fundamental properties create a whole new set of tradeoffs that were previously unattainable.

General Form of Chord™ Signaling

One of the main innovations behind Kandou's Chord™ signaling is the use of correlated signalis on multiple wires. For a fixed number of wires, also called the "interface size", correlated signals, rather than independent signals, are sent across the wires, as shown in the figure on the right.



The incoming bits (1) are fed into a digital encoder (2) that transforms the incoming bits into N pieces of information that are forwarded to the ensemble driver. The analog ensemble driver (3) puts signals across each of the N wires of the interface. We often use the terminology "NbMw" to describe the most fundamental property of a Chord™ signaling method: (N) is the number of raw data bits per symbol time (b) to be delivered across an interface; and (M) is the number of wires (w) over which the code is delivered. For example, a 5b6w interface sends five bits per symbol time over 6 wires. The ensemble driver may be combined with other circuitry, such as pre-emphasis circuit or a FIR filter in order to assist the equalization process.

The multiwire channel (4) carries the signals from the transmitter to the receiver. This channel must be constructed to have low skew amongst the wires. The skew requirement amongst these wires is of the same order as the intra-pair skew requirement of differential signaling.

The signals from the channel are input to an ensemble receiver (5). The task of the receiver is to coherently detect the signals on the wires. The ensemble receiver may contain circuitry for further equalization of the signals, and for tasks such as clock and data recovery (CDR). The ensemble receiver typically consists of analog circuits. The ensemble receiver creates information for the decoder (6), typically a piece of digital logic, to re-create the original bits (7). When some of the simplest Chord™ signaling methods are employed, the digital decoder is absent because the decoding can be performed by special analog circuits residing in the ensemble receiver.

Central to Chord™ signaling is the concept of a chordal code. The codebook of the chordal code consists of the set of all vectors obtained from the values that are simultaneously transmitted on the wires.

Excluding our CMOS solution, the wires in Kandou's interfaces have a common termination. The signals on these wires are balanced through the careful design of our codes. This means that on the interface as a whole the amount of current flowing in one direction is equal to the amount flowing in the other direction. This has many advantageous properties, as it makes the transmission immune to simultaneous switching output (SSO) noise. Kandou's ensemble receivers are reference-less, making them immune to common mode noise on the wires. The ensemble drivers can be implemented as either current mode (CML) or voltage mode (VML), just as differential drivers can be. The ensemble receivers achieve signal integrity improvements similar to what differential receivers achieve compared to single-ended receivers. Because of these improvements, the swing of the signals can be reduced, and with that also the line power consumption. This reduction is only one of the ways that Kandou's solutions reduce power consumption.

For the most challenging and highest speed links, Kandou's Ensemble NRZ interface directly generalizes differential NRZ signaling onto a four-wire link that carries three NRZ inputs. Ensemble NRZ employs a linear transform, allowing a flexible combination of analog and digital implementations.

The greatest gain when using Chord™ signaling is obtained by matching the channel with the optimal code choice and transceiver architecture.

Kandou's Codebooks

The signals carried over the multiwire bus belong to a well-designed "codebook" underlying the chordal code. A codebook, or a code, is a collection of vectors (also called codewords) in which each component belongs to a fixed alphabet. For example, the code corresponding to differential signaling consists of the codewords (+1,-1) and (-1,+1). The bit to be transmitted determines which of the codewords is to be sent on the two wires. In the same way, a different chordal code underlies each of Kandou's Chord™ signaling techniques. The task of the encoder is to pick one of the codewords upon receiving the input bits. The codeword determines the values to be sent on the wires, and a new codeword is transmitted every unit interval (UI).

Kandou's chordal codes are designed with several goals in mind:

(a) Efficient encoder logic, typically a digital implementation,

(b) Efficient driver circuitry, typically an analog/mixed-signal implementation,
(c) Efficient receiver circuitry, typically an analog/mixed-signal implementation,
(d) Efficient decoder logic, typically a digital implementation,
(e) Increased immunity against various types of noise, such as common mode noise, SSO, thermal noise,
(f) Increased pin-efficiency (ratio of bits transmitted per clock cycle and the number of wires in the interface),
(g) Decreased power consumption.

Because of the underlying coding technology, Kandou offers a whole class of new signaling methods and opens a new field in the area of signaling for high-speed buses.

Kandou's Specific Chord™ Signaling Techniques

There are a large number of possible choices for the design of codes and associated interfaces. These interfaces offer many tradeoffs in terms of their size, required speed, required static & dynamic power consumption, final bit error rate, tolerance to channel attenuation, tolerance to various types of noise impairments, support for Decision Feedback Equalizers (DFEs), type of the driver (CML/VML or CMOS-like), power-down modes, and footprint.

Among these, Kandou Bus has identified five distinct chordal codes that cover a large variety of applications. The full links implementing these codes are called "interfaces."

(a) **The CMOS interface:** ideal for links with CMOS drivers to lower the SSO noise and lower the dynamic power consumption while keeping the static power consumption low.
(b) The 5b6w interface: ideal for highly latency sensitive, short chip-to-chip links across an interposer, or across dies in the same package where single ended signaling has signal integrity issues and differential is too costly w.r.t. pin count and power consumption.
(c) The 8b9w interface: ideal for fairly latency sensitive, short (up to 10cm) chip-to-chip links not requiring heavy equalization.
(d) The 8b8w interface: a fully pin-efficient interface usable across a wide range of chip-to-chip interconnects with channel attenuations down to -15 dB.
(e) The Ensemble NRZ (ENRZ) interface: ideal replacement for differential signaling across a wide range of channel conditions, especially those that require DFEs.

	CMOS	5b6w	8b9w	8b8w	ENRZ
LINK LENGTH	< 5mm	1-20 mm	5 mm - 10 cm	5mm - 30cm	>20 cm
INTERFACE SIZE IN WIRES	> 2	6	9	8	4
BITS PER WIRE	1 - 1.5	5/6	8/9	1	3/4
LINE POWER	1/4	2/5	1/4	1/4	1/3

All of Kandou's interfaces other than the CMOS interfaces have CML/VML drivers. All of these interfaces have been designed with specific applications in mind, which we will elaborate on later in the document. Some of these interfaces (such as the ENRZ) interface has been designed to withstand very demanding channel conditions while allowing higher throughput. Others are designed for applications where heavy equalization is not required, but the speed of the data transfer and the associated power consumption are of utmost importance. All of our interfaces have a pin-efficiency (bits per wire) larger than the bits per wire of differential signaling, which is 1/2, meaning that they need fewer wires to transmit the same amount of data. The following table summarizes some of the basic properties of these interfaces:

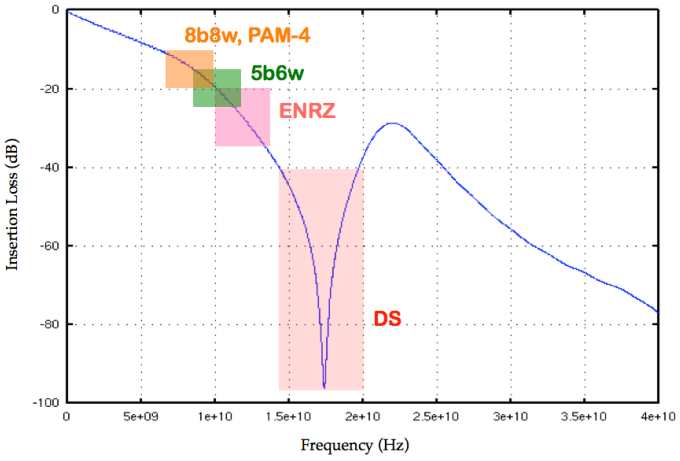
In all cases except the CMOS case, line power is in comparison with differential signaling. In the case of the CMOS driver the line power is measured in comparison with a conventional CMOS driver.

How Does Chord™ Signaling Save Power?

Kandou's Chord™ signaling leads to lower power per delivered bit at a given speed when compared to competing interfaces based on standard differential signaling or, in one case, to CMOS/single ended drivers. Lower power per delivered bit means higher overall throughput, equal throughput at lower power, or a combination of these.

The lower overall power consumption is due to the combination of a number of factors: lower line power, lower power needed for clock and data recovery, lower clock rates leading to less power used for equalization, and the simplicity of the receiver which does not require external references. For our non-CMOS interfaces, some of the advantages of Chord™ signaling techniques leading to lower power are given below.

(a) **Lower clock rates:** Compared to interfaces based on differential signaling, Kandou's interfaces can lower the clock rate considerably to achieve the same overall throughput. This often leads to lowering the channel attenuation (and with that the need for advanced and expensive equalization techniques), and to easier CDR circuits, which again lead to lower overall power consumption. The pin-efficiency of the interface is a proxy for how much the clock rate can be reduced. For example, a pin-efficiency of 1 reduces the clock rate by a factor of 2 as compared to differential signaling, whereas a pin-efficiency of 0.75 reduces the clock rate by a factor of 2/3. As an example, consider a channel with the loss characteristics given in the figure below.. A differential signaling scheme with symbol rates in the range 28GBaud to 40GBaud will suffer extreme channel loss (indicated by the purple rectangle entitled "DS") for which the required equalization will be very expensive to implement. By using a Kandou code to operate with an equivalent throughput at a lowered symbol rate of 14GBaud to 20GBaud per wire, the channel loss is reduced by many dBs, which allows significantly improved performance and reduces equalization complexity.



(b) **Lower line power:** Because of the coding, at the same peak-to-peak voltage level, Kandou's interfaces have a lower average current flow per wire than interfaces based on differential or single-ended signaling. For example, the 5b6w interface uses the current needed for two differential lanes and distributes it among 6 wires to deliver 5 bits. As a result, the line power of this interface, as compared to differential signaling, is 2/5, or 40%. Similarly, the 8b8w interface uses the current needed for just two differential lanes and distributes it among 8 wires to deliver 8 bits. As a result, it saves 75% line power compared to 8 differential lanes needed to deliver the 8 bits. The line power efficiencies of Kandou's interfaces are given in the above table.

(c) **Clock and Data Recovery (CDR):** CDR is one of the highest power consuming parts of high-speed serial links. Typically, when differential signaling is used, CDR is performed across the two wires making up a differential link. Since Kandou's interfaces are generalizations of interfaces based on differential signaling, a joint CDR is performed across all the wires making up the interface. As a result, the power used by the CDR unit is amortized across all the bits delivered by the interface, thereby reducing the power required for the delivery of each bit.

(d) **Simple receiver**: While other techniques such as using PAM-4 signaling, can also lower the channel bandwidth requirements, these interfaces are more complicated in terms of the receiver structure. Some of these techniques in-

cluding PAM-4 also have inferior ISI tolerance and as such need enhanced equalization techniques. In contrast to PAM-4 architectures, Kandou's receivers are completely self-referenced. Therefore, there is no need for the regeneration of a reference, or for circuitry to mitigate the noise associated with such a reference. Moreover, the DFEs that can be used with the ENRZ code are simpler than those needed for PAM-4 because ENRZ delivers NRZ eyes to the DFE. This allows the critical unrolled portion of a DFE to work with just two levels instead of four. The combination of these advantages leads to tangible reductions of power of Kandou's interfaces when compared to competing technologies.

	TECHNOLOGY	ATTENUATION	SPEED	POWER
CMOS	25 nm DRAM*	< 2 dB	400 Mbps/pin	< 0.3 pJ/bit**
5b6w	TSMC 40 GP*	< 3 dB	8 Gbps/pin	< 0.3 pJ/bit
5b6w	TSMC 40 GP*	< 5 dB	16 Gbps/pin	< 0.5 pJ/bit
ENRZ	TSMC 28 HPM*	< 35 dB	21 Gbps/pin	< 10 pJ/bit
8b8w	TSMC 40 GP***	< 20 dB	16 Gbps/pin	< 4 pJ/bit
8b8w	UMC 90***	< 10 dB	6 Gbps/pin	< 2 pJ/bit

Exactly how much Kandou's interfaces save power compared with competing technologies depends on a number of parameters. As an example, Kandou's TSMC 40nm GP demonstrator implementation of the 8b8w interface for a channel of the type given above uses in total less than 4 pJ/bit for transmission at 16 Gbps/wire. An interface based on differential signaling on this channel would use significantly higher power due to the very high channel attenuation. Circuit level simulations of Kandou's 5b6w interface for communication across a few mm of copper lead to a power consumption of less than 0.3 pJ/bit at a speed of 8Gbps/pin when implemented in TSMC 40nm GP. When going faster, at double that speed per pin, the power consumption increases slightly to 0.5 pJ/bit. All these numbers are very competitive with the highest reported in the literature.

Applications of Kandou's Interfaces

* Circuit level simulations ** Line power *** Silicon available

	BACKPLANE LINKS	MEMORY I/O	SHORT LINKS	INTER-PACKAGE LINKS	CABLES	TSV
CMOS						X
5b6w	X		X	X		
8b9w		X				
ENRZ	X				X	
8b8w	X	X				

Networking applications: The Ensemble NRZ interface is an ideal solution for networking applications as it allows for the use of DFEs, which are needed when the communication channel consists of multiple boards and connectors that produce reflections. ENRZ carries three NRZ channels over four wires. Compared to NRZ at the same clock rate, ENRZ

increases the throughput by a factor of 1.5, and reduces the line power by a factor of 3. Moreover, since the ENRZ interface can be switched to work in differential mode if needed, it can be used in legacy applications. In situations where DFEs are not needed, other Kandou interfaces such as the 5b6w interface or even the 8b8w interface can be used to increase the data throughput even further to 1.66 times and 2 times the throughput of NRZ, respectively.

Transmission on cables: Data transmission on cables at high speeds requires a number of mitigating techniques to guarantee signal integrity in the face of channel impairments such as ISI. Moreover, since the signaling used needs to cause very low electromagnetic interference (EMI) as such noise can adversely affect other electronic equipment nearby. The ENRZ interface is an ideal replacement for techniques based on differential signaling (such as Low Voltage Differential Signaling -- LVDS) because ENRZ increases the throughput of the link while guaranteeing signal integrity and very low electromagnetic emissions.

Packaging and Interconnect: Several of Kandou interfaces are ideal for optimizing interconnect in modern semiconductor package and interconnection technologies. Kandou's interfaces will support wire-bond, flip-chip, micro-bump, through-silicon-vias (TSVs) and interposer technologies. Wire-bond and flip-chip packages are typically used in ASIC and catalogue products. Micro-bump, TSV and interposer technologies are commonly used in memory components and high-density applications such as mobile. With high pin efficiency the total number of circuit pins in an interface may be reduced, giving a smaller physical interface size and hence lowering package and/or assembly costs. The lower signal rates on the wires contribute to lower losses in the serial link.

Kandou Silicon

Kandou Bus has developed a silicon demonstrator of the correlated coding technology. An 8b8w transceiver known as FireFly40 has been implemented in TSMC 40nm GP technology. The transceiver includes:

- Transmit features include a 8b8w encoder, serializer, multiwire driver and 1 tap FIR equalizer.
- Receive features include a CTLE equalizer, samplers, per-wire de-skew circuit, deserializer, data detection and aligner, 8b8w decoder.

Link speed	8 - 16 GTps
Channel attenuation	<20 dB at Nyquist 8 GHz
Link architecture	8b8w
Equalization	CTLE and 1-tap Tx FIR
Offset correction	Yes
BER	$<10^{-12}$
Differential legacy mode	Yes, optional
De-skew capability	1 UI per wire
Power efficiency	< 4 pJ/bit, Vdd = 0.9V

Test features include a transmit pattern generator, receive error checker, receive eye scope, and loopbacks.

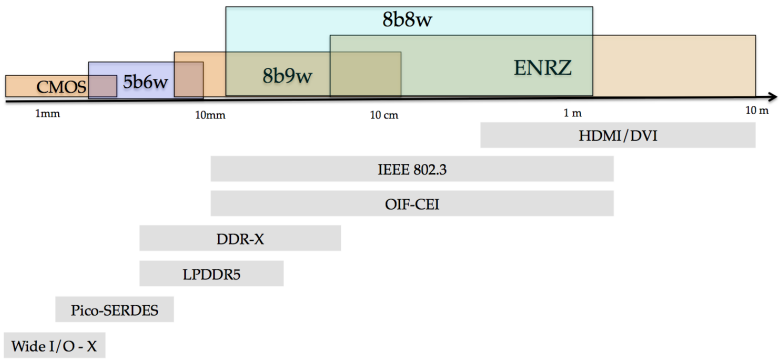
- Control features include a SPI interface.and access to extensive internal state information.
- Compatibility features include a differential mode.

The key specifications of the FireFly40 demonstrator are given in the table on the right.

Standards

Kandou's interfaces are applicable to a wide range of chip-to-chip communication links and can drastically reduce the power consumption, and increase the speed of such links. As a result, they are good candidates for standardization. Because of their versatility, they can be used in a variety of standards, from those regulating communications across tiny links to those responsible for communication over long cables.

The figure on the right gives a rough mapping of Kandou's various interfaces to several standards. Our single-ended CMOS links can be adopted by various Wide I/O standards as they relate to lowering the SSO noise and the power consumption of communication across multiple stacked dies. Our 5b6w interface can be applied to the new and upcoming Pico-SERDES standard. The 8b9w interface is ideal for future generations of the LPDDR and the DDR standards, due to its low power and support for very high speeds. The 8b8w and the ENRZ interfaces are ideal for various OIF-CEI and IEEE 802.3 standards. For example, the ENRZ interface has been proposed by Kandou Bus as a candidate for several draft standards. Links requiring heavy equalization, for example cable links encountered in HDMI and DVI standards, can benefit greatly from the ENRZ interface as this interface can increase the throughput of the link by as much as 50% while maintaining industry standard signal integrity.



About Kandou Bus

Kandou Bus (http://www.kandou.com) is a fabless semiconductor IP company specializing in the design of high-speed, pin-efficient, energy-efficient serial links, SerDes, and associated technologies based on correlated data coding and signaling techniques. Kandou Bus follows an IP business model with three typical elements of non-recurring engineering revenues for custom work, and licensing fees/royalties in case of productization.

Kandou Bus has development centers in Switzerland and the UK.

For more information please contact info@kandou.com.