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KANDOU 500GBPS SERDES IP TARGETS 2.5D

By Bob Wheeler (September 11, 2017)

Kandou's new 16nm Glasswing hard macro enables 500Gbps interfaces between die in a 2.5D package. Like its 28nm predecessor (see *MPR 3/30/15,* "Kandou Narrows Focus to Serdes IP"), the new intellectual-property (IP) core implements the company's CNRZ-5 protocol for 5-bit over 6-wire signaling. Whereas the older GW28-125-USR instantiates one such serdes, however, the new GW16-500-USR has four. Kandou is characterizing a 500Gbps test chip in its lab and plans to complete qualification of its IP by the end of the month.

The new core is arriving as the small company grows in both headcount and customer engagements. In 2016, Kandou raised its first venture funding: $15 million, led by Bessemer Venture Partners. It has more than 45 employees and expects to exceed 70 by year-end. Kandou's first announced customer is Marvell, which licensed Glasswing for use in its MoChi designs (see *MPR 1/11/16,* "MoChi Expands Marvell's Armada"). In addition to the Glasswing hard IP, the company licenses its IP to address other process technologies and interface widths. It's also developing custom silicon incorporating its IP for multiple customers. The company has filed more than 200 patents to protect its technology.

The GW28-125-USR and GW16-500-USR both operate at 25Gbaud, or 12.5GHz. After coding overhead, CNRZ-5 yields 125Gbps of effective bandwidth at that baud rate. This approach compares with using five differential pairs, or 10 wires, to deliver the same bandwidth using NRZ coding. Glasswing's core-side interface is 160 bits wide and operates at 780MHz. The IP blocks include a differential clock that's forwarded between the CNRZ-5 transmitter and receiver, eliminating the need for clock/data recovery (CDR). The four CNRZ-5 serdes in the 500Gbps core share a single clock. All told, a 500Gbps design requires 52 wires (24+2 each way).

The first GW16-500-USR variant targets the TSMC 16FF+ process; Kandou says it will port the core to 16FFC in 4Q17. Because it's intended for die-to-die connections in a 2.5D package, the core is designed for channels of only 24mm or less. This ultra-short-reach channel allowed the company to optimize for low power combined with a low bit error rate (BER) of 10^{-15}. The 16nm test chip consumes 800mW, which equates to 0.82pJ per bit. The hard macro's 150-micron bump spacing limits its area to 2.4mm by 1.0mm.

Kandou's test chip has achieved its target BER on channels of various shapes and lengths, including a 30mm one without any turns of 90 degrees or greater. To handle difficult channels, add margin, or reduce power (using smaller voltage swings), the company now offers optional forward-error-correction (FEC) IP. Because of Glasswing's low BER, the FEC code is short; it adds only 1.28ns to Glasswing's fixed latency of less than 4ns.

Although Kandou has customer programs that span several end markets, the GW16-500-USR's main target is connecting a network ASIC die to a separate 56Gbps PAM4 serdes die (or "chiplet"). For example, the core could link a 400G Ethernet MAC/PCS block to 8x56Gbps PAM4 serdes on a separate die. (Owing to network-FEC overhead, which is added in the PCS layer, the serdes interface may require nearly 450Gbps of bandwidth.) By separating most digital logic from the network transceivers, chip designers can employ leading-edge process technology (e.g., 7nm) for the Ethernet MAC/PCS block while using a lower-cost technology for the PAM4 serdes blocks.

Other GW16-500-USR applications include linking a processor or ASIC to an on-chip optical engine and linking multiple CPU die in a multicore SoC. The GW28-125-USR can connect a wireless baseband to an RF module, connect an image sensor to an image processor, or perform a similar lower-speed task. To minimize power, designers can reduce clock speed to match their required bandwidth. The company says it has customers across all of the aforementioned applications.

For Kandou, the great advantage of on-chip interconnects is that they don't require standards. Typically, one customer controls both ends, enabling the use of new and unusual protocols such as CNRZ-5. These applications also require low power per bit, as multidie approaches can't add much power compared with monolithic designs. Finally, some of these designs require high bandwidth, measured in terabits per second. The market is coming to Kandou, more than six years after its founding, through volume adoption of 2.5D packaging. ♦

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