# Glasswing - GW16-500 SerDes

*A set of programmable IPs designed and optimized for in-package applications*

## Description

The Glasswing SerDes family is a set of programmable IPs designed and optimized for in-package applications. Glasswing provides high system bandwidth with low power consumption through the use of CNRZ-5-DR-EE Chord™ signaling and a forwarded clock architecture. Glasswing IP may be deployed in multiple instances to provide efficient extended interfaces.

## Technology

- TSMC 16 nm FF+-GL process
- 0.9V analog, 1.1V HV analog, and 0.8 V or 0.85 V digital supplies
- Junction temperature -40 to +110 °C
- Standard flip chip technology
- Tile-able layout to support high IO density

## Deliverables

- Datasheet and application notes
- Standard integration views: GDSII, SDC, LEF, Verilog, .lib
- Reference models and test benches
- Qualification report
- Package design and integration guidelines
- Testability and manufacturing guidelines
- Evaluation modules

## Availability

For sample availability, contact us at sales@kandou.com or via our contact page at www.kandou.com/contact/.

## Features

- Data is 5b6w encoded
- Four groups of five 32 bit RX and TX parallel buses
- 125 Gb/s over each group of six wires; total throughput of 500 Gb/s in each direction
- Has a common block with PLL and references
- DC coupled link requiring no data coding or scrambling
- Internal TX to RX loopback
- Programmable TX swing; maximum 300 mVpp single-ended
- CTLE RX equalization
- Timing delivered via a forwarded clock and a Clock Data Aligner (CDA) circuit.
- Programmable RX CDA coefficients
- EyeScope (non-destructive)
- Rate is variable from 250 Gb/s to 500 Gb/s through RefClk and PLL control
- RX bit-slipping control for word alignment
- PRBS15 and PRBS31 pattern TX generation and RX verification, plus a user defined pattern
- DFT: at-speed BIST of analogue plus stuck-at scan of slow digital circuitry
- Supports JTAG boundary scan (1149.1) and scan test modes
- Analog test port
- ATPG support
- APB (ARM Peripheral Bus) interface for easy programming and integration plus a simpler mode
- Compatible to the JEDEC JESD247 Multi-wire Multi-level Interface Specification

## Applications

- Multi-chip modules and short reach interposers:
  - Packaging dies with dissimilar foundry processes
  - Packaging of smaller dies to increase yield
- High throughput data interfaces:
  - Efficient interface to off-board SerDes tiles
  - Interconnection of tiled CPUs or DSPs
  - Processor or switch to high bandwidth
  - memory
  - Efficient interface to optics engines
    Switch-to-switch links

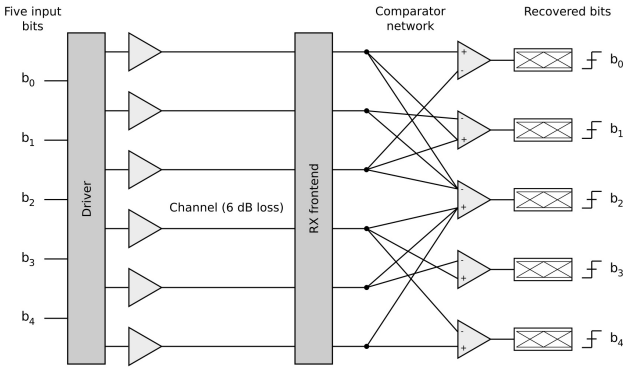
## Advantages

- 2-4x throughput at 50% or less energy consumption as compared to conventional SerDes over the same number of pins/wires
- High pin-efficiency and low power
- 417 Gb/s/mm bidirectional data throughput
- Supports up to 6dB channel insertion loss at 12.5 GHz
- NRZ-like Inter-Symbol Interference (ISI) performance
- NRZ-like EMI, SSO and balance properties

## Glasswing 5b6w Coding

- Transmits 5 bits on 6 wires:
  - Has a zero SSO transmitter
  - Employs a reference-less receiver that is resilient to common-mode noise
  - Uses a receiver that has 5 comparators and no decoder
- Link has excellent signal integrity properties:
  - NRZ-like Inter-Symbol Interference properties
  - Scalable to much higher speeds and harder channels
  - NRZ-like EMI performance

## Coded Link Block Diagram




## Simplified Schematic