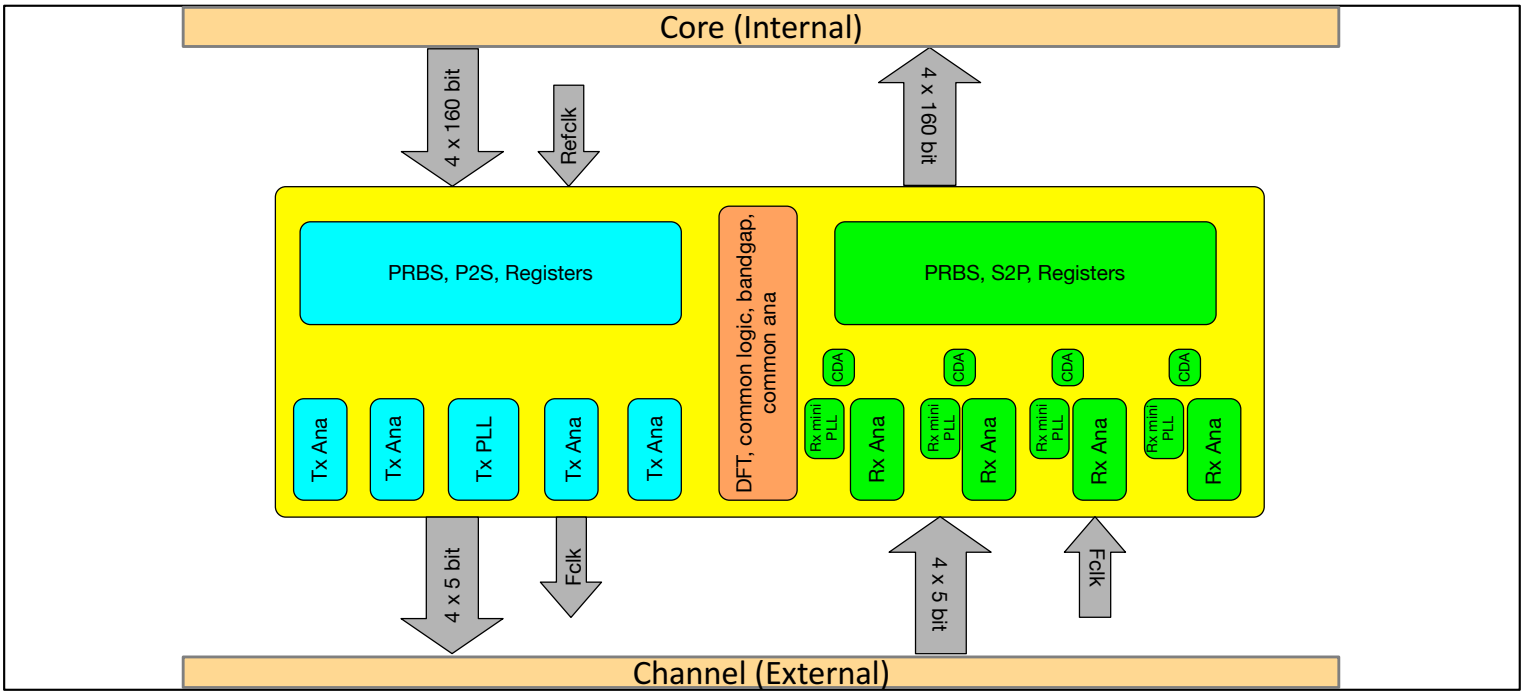
KANDOU BUS

Glasswing™ IP Family
Preliminary

GW-500 SerDes
500Gb/s Throughput



Description:

The Glasswing™ SerDes family is a set of programmable IPs designed and optimized for in-package applications. Glasswing provides high system bandwidth with low power consumption through the use of 5b6w Chord™ signaling and a forwarded clock architecture. Glasswing IP may be deployed in multiple instances to provide efficient extended interfaces.

The GW-500 SerDes is a hard IP solution that delivers 500Gb/s of bi-directional throughput at <1.0pJ/bit and is ideal for both ultra-short reach organic substrate and interposer applications on multi-chip-modules.

The GW-500 achieves low power through coding, efficient circuitry, and simple clocking and equalization schemes.

Advantages:

- 2-4X throughput at >50% energy savings vs conventional SerDes
- No interposer required
- Double-stackable
- High pin-efficiency, low power, and low fixed latency
- 417Gb/s/mm bidirectional data throughput
- Supports up to 6dB channel insertion loss at 12.5GHz
- NRZ-like Inter-Symbol Interference (ISI) performance
- NRZ-like EMI, SSO and balance properties

Features:

- Data is 5b6w encoded
- Four groups of five 32-bit Rx and Tx parallel busses
- 125Gb/s over each group of 6 wires; total throughput of 500Gb/s in each direction
- Has a common block with PLL and references
- DC coupled link requiring no data coding or scrambling
- Internal Tx-to-Rx loopback
- Programmable Tx swing; maximum 300mVpp single-ended
- CTLE Rx equalization
- Timing delivered via a forwarded clock and a Clock Data Aligner (CDA) circuit
- Programmable Rx CDA coefficients
- EyeScope (non-destructive)
- Rate is variable from 250Gb/s to 500Gb/s through RefClk and PLL control
- Rx bit-slipping control for word alignment
- 1e-15 BER (1e-20 BER with optional FEC)
- PRBS15 and PRBS31 pattern Tx generation and Rx verification, plus a user defined pattern
- DFT: at-speed BIST of analog plus stuck-at scan of slow digital circuitry
- Supports JTAG boundary scan (1149.1) and scan test modes
- Analog test port
- APB (ARM Peripheral Bus) interface for easy programming and integration plus a simpler mode.
- Compatible to the JEDEC JESD247 Multi-wire Multi-level Interface Specification

Kandou Bus S. A., QI-I, 1015 Lausanne, Switzerland
email: sales@kandou.com
web: www.kandou.com

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Technology:
- TSMC 16nm FF+-GL-12LM process
- 0.9V analog, 1.1V HV analog, and 0.8V or 0.85V digital supplies
- Junction temperature -40 to +110 degrees C
- Standard flip chip technology
- Tile-able layout to support high IO density

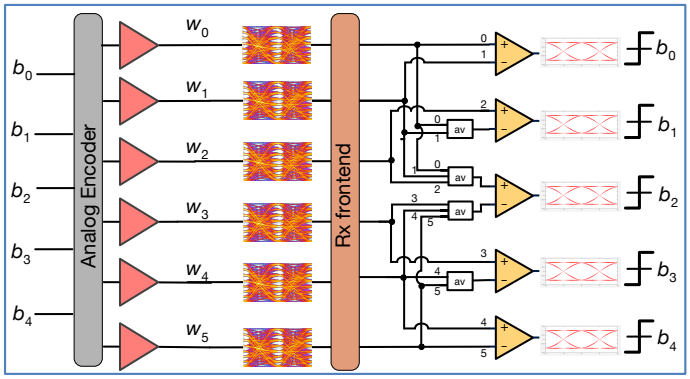
Applications:
- Multi-chip modules and short reach interposers:
  - Packaging dies with dissimilar foundry processes
  - Packaging of smaller dies to increase yield
- High throughput data interfaces:
  - Efficient interface to off-board SerDes tiles
  - Interconnection of tiled CPUs or DSPs
  - Processor or switch to high bandwidth memory
  - Efficient interface to optics engines
  - Switch-to-switch links

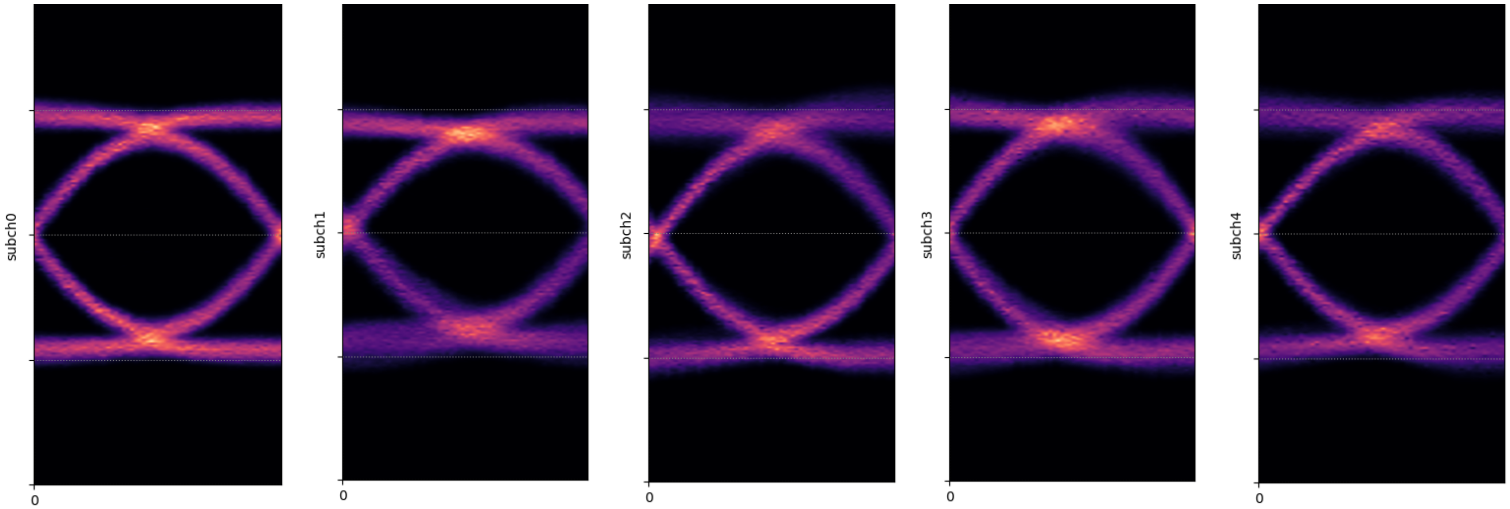
Deliverables:
- Data Sheet and Application notes
- Standard Integration Views: GDSII, SDC, LEF, Verilog, .lib
- Reference Models and Test benches
- Qualification Report
- Package Design and Integration guidelines
- Testability and Manufacturing guidelines
- Evaluation Modules

Availability:
- For sample availability and pricing, contact Kandou Bus (*sales@kandou.com*)

Related Material:
- *http://www.kandou.com/documents*

Glasswing 5b6w Coding:
- Transmits 5 bits on 6 wires:
  - Has a zero SSO transmitter
  - Employs a reference-less receiver that is resilient to common-mode noise
  - Uses a receiver that has 5 comparators and no decoder
- Link has excellent signal integrity properties:
  - NRZ-like Inter-Symbol Interference properties
  - Scalable to much higher speeds and harder channels
  - NRZ-like EMI performance





Glasswing measured sub-channel transient eyes at 25 GBaud for an MCM channel at 12.5GHz.