Chord Signaling for High Bandwidth Extra Short Reach Interfaces

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Executive Summary

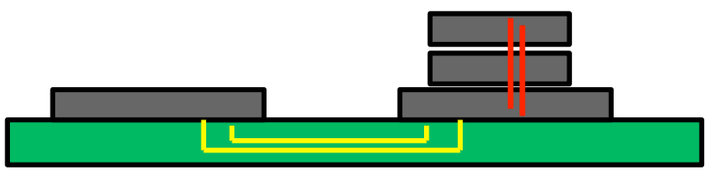
- An emerging class of applications uses extra short reach interfaces (less than 5cm) over silicon substrate to connect high density ASIC chips with Optical Engines and/or DRAM chips.
- High Speed I/O solutions optimized for this application space can offer significant power savings over generic Serdes devices.
- These charts describe a High Speed I/O solution based on Chord signaling Glasswing 5b6w code.
  - Power of 0.38 pJ/bit is achievable with this technology.

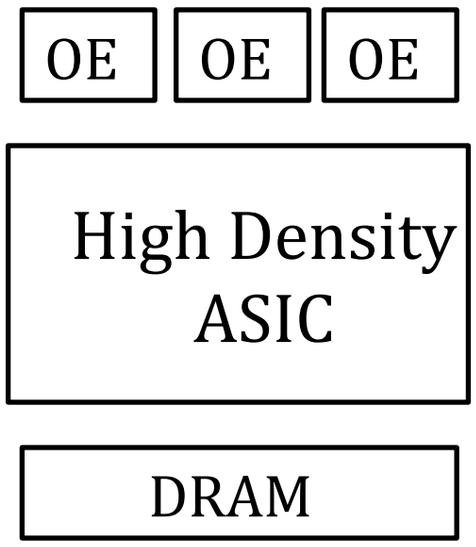
Kandou Bus Glasswing 5b6w Advantages
as compared to NRZ and PAM-4

- 67% better pin efficiency than NRZ:
  - NRZ: 1 bit over 2 wires = 0.50 bits per wire
  - Glasswing 5b6w: 5 bits over 6 wires = 0.83 bits per wire
- 50% better eye launch amplitude than PAM-4:
  - PAM-4 Eye: 33% of dynamic range
  - GW 5b6w Eye: 50% of dynamic range (worst case)
- 33% less ISI than PAM-4:
  - PAM-4 ISI Ratio* : 3
  - GW 5b6w ISI Ratio* : 2 (worst case)
- 60% less driver line power than NRZ:
  - Glasswing 5b6w total drive current on 4 wires is 40% of the drive current on an equivalent NRZ interface consisting of 5 differential pairs.
- 30% fewer wires than NRZ at same baud rate.
  - GW 5b6w x 2 channels (192 Gb/s):
    28 wires - (12) Tx + (12) Rx + (4) clock
  - NRZ 20 lanes @ 19.2 Gbaud/s:
    40 wires - (20) Tx + (20) Rx

* ISI Ratio is the ratio of larger eye over smallest eye as measured at Rx comparator(s), and is a useful predictor of the impact of ISI on eye closure inherent in an architecture. Larger ratios indicate more ISI which will result in more horizontal eye closure.

Application Space





- High Density technologies:
  - 2.5D technology integrates multiple chips on a silicon substrate
  - 3D technology stacks chips interconnected using Thru-Silicon Vias (TSVs)
- Applications include connecting high density ASIC chips to optical engines or DRAM chips (which may be stacked).
- Extra short reach channels for these applications are < 5 cm with minimal impedance discontinuities.
- Interface technologies optimized for these channels can significantly reduce power consumption.

Definition of Chord Signaling

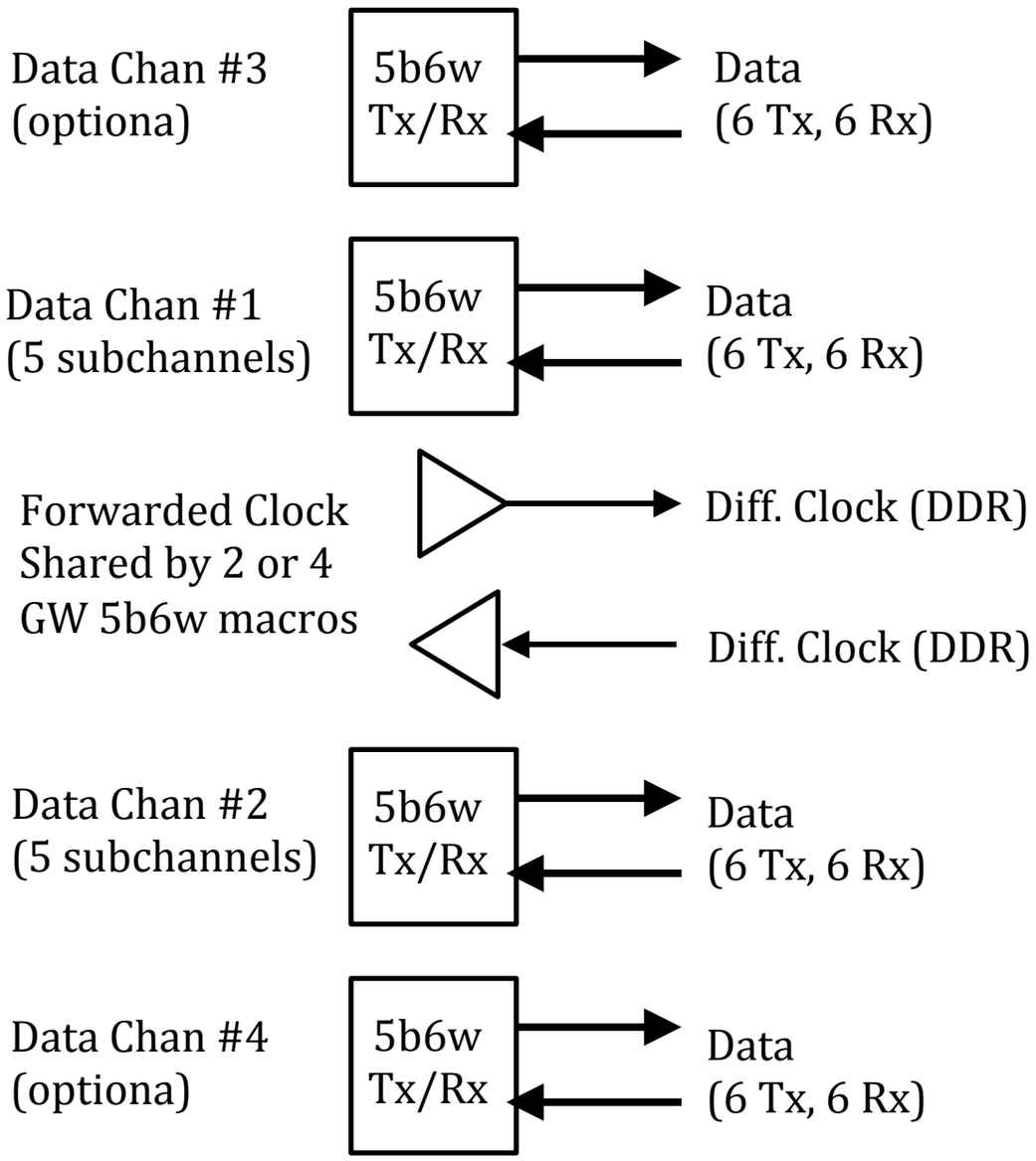
- Chord signaling consists of various signaling codes with the following properties:
  - Data channel consists of N wires where N ≥ 2.
  - The sum of voltages over all wires equals a constant.

- The Glasswing class of Chord signaling codes uses ternary signaling to reduce driver line power.
  - Each ternary driver is in either a +1, 0, or -1 drive state.
  - Glasswing codes drive subset of wires to +1/-1 states.
    - Drivers at 0 state do not contribute to line power.
  - Glasswing code density (bits/wire) is significantly higher than an equivalent implementation using NRZ differential pairs.
  - Combining higher bit densities and utilization of ternary states results in a substantial reduction in driver line power when compared to an equivalent NRZ interface.

Glasswing 5b6w Code Description

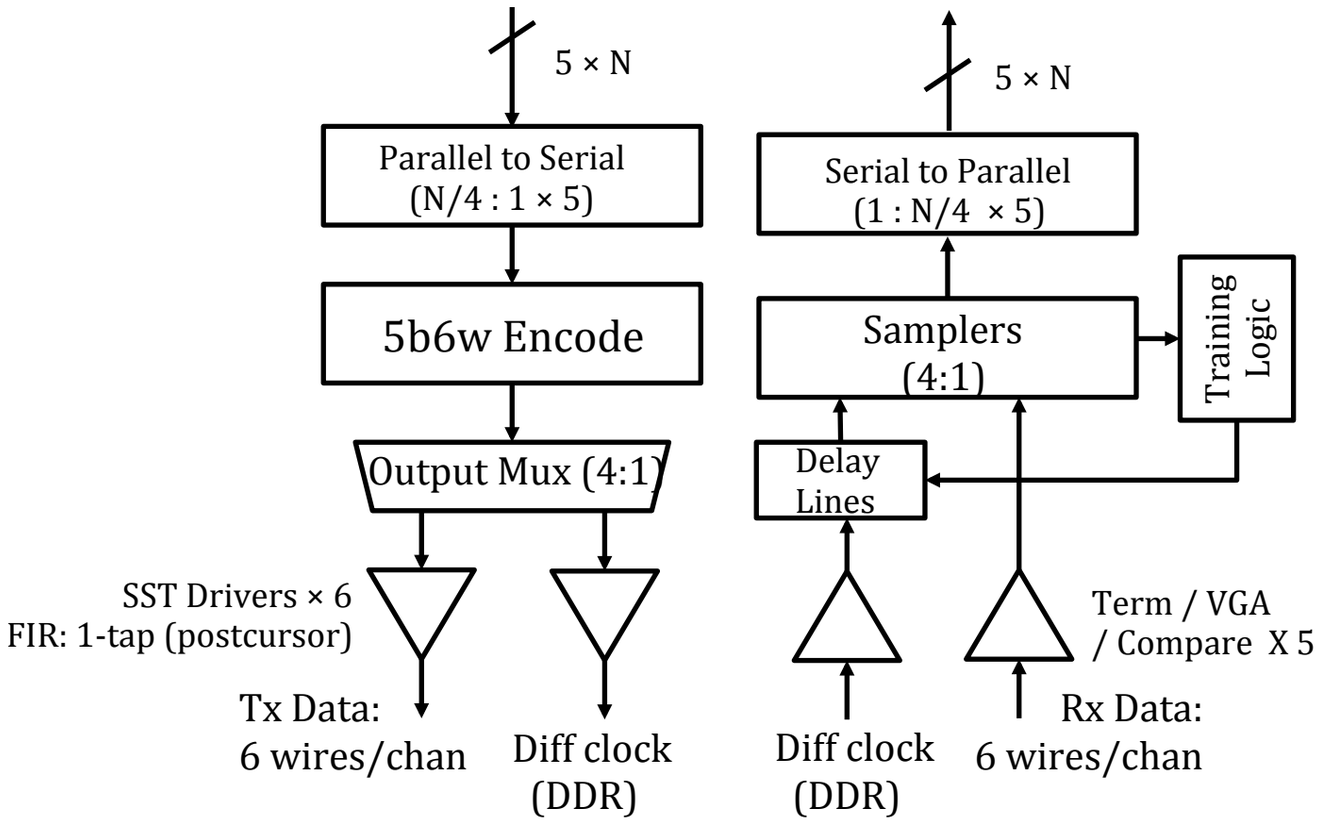
- Glasswing 5b6w code is a ternary code that encodes 5 bits per baud symbol.
- Code book consists of permutations of: (+1, +1, 0, 0, -1, -1)
  - Total of 32 code words used to encode 5 bits of data.
- V_{CM} is a constant (sum of state values for all code words is zero).
- Receiver differentially decodes each sub-channel by combining inputs.
- Decode is performed directly by comparators; no logic decode stage is needed.

Glasswing 5b6w Architecture for Short Interfaces



- Each data channel is:
  - 5 Tx, 5 Rx subchannels
  - Coded on 6 Tx, 6 Rx wires
- Forwarded DDR clock (differential)
  - Shared by up to 4 channels
  - No CDRs needed

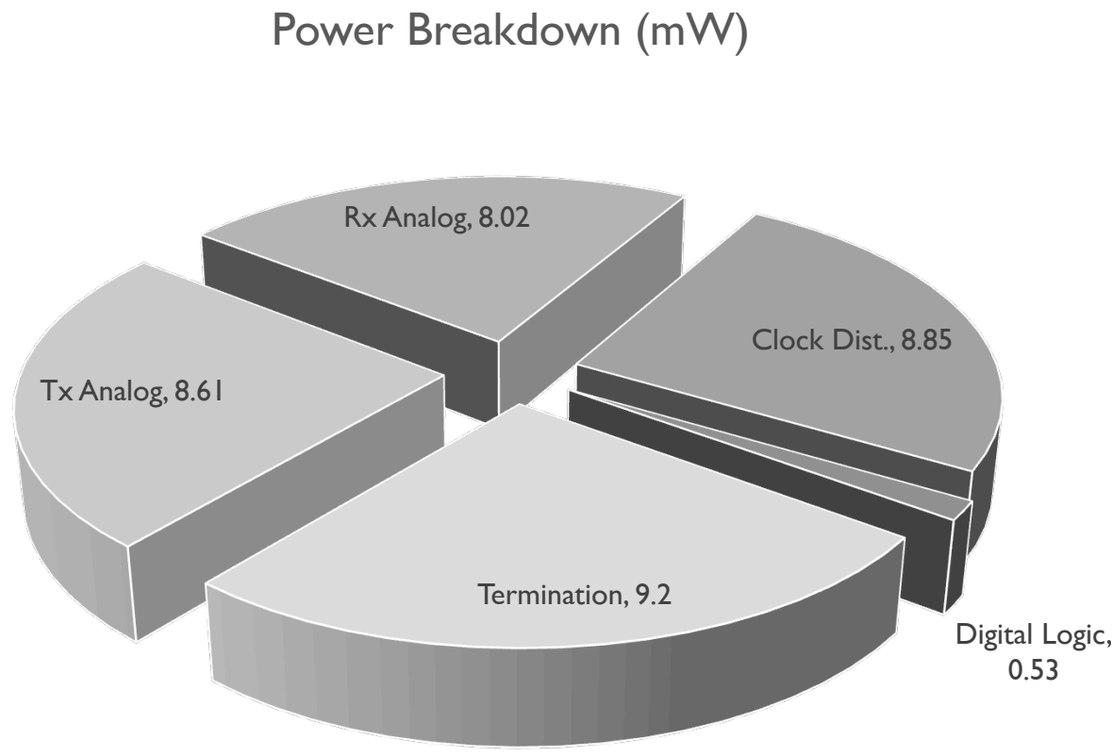
Glasswing 5b6w Macro Architecture



- 6 Tx , 6 Rx data wires/chan.
- Forwarded diff. DDR clock (shared).
- Core side interface: 5N bits each direction.
- Simple signal processing:
  - 1-tap FIR (postcursor)
  - No DFE, CDR, CTLE.
  - No PLL; chip-level PLL supplies low jitter clock.
- Tx launch: 200 mVppd
  - 400 mVppd for channels with reflection issues
- Rx training logic centers clocks to samplers

Power Estimate @19.2 Gbd

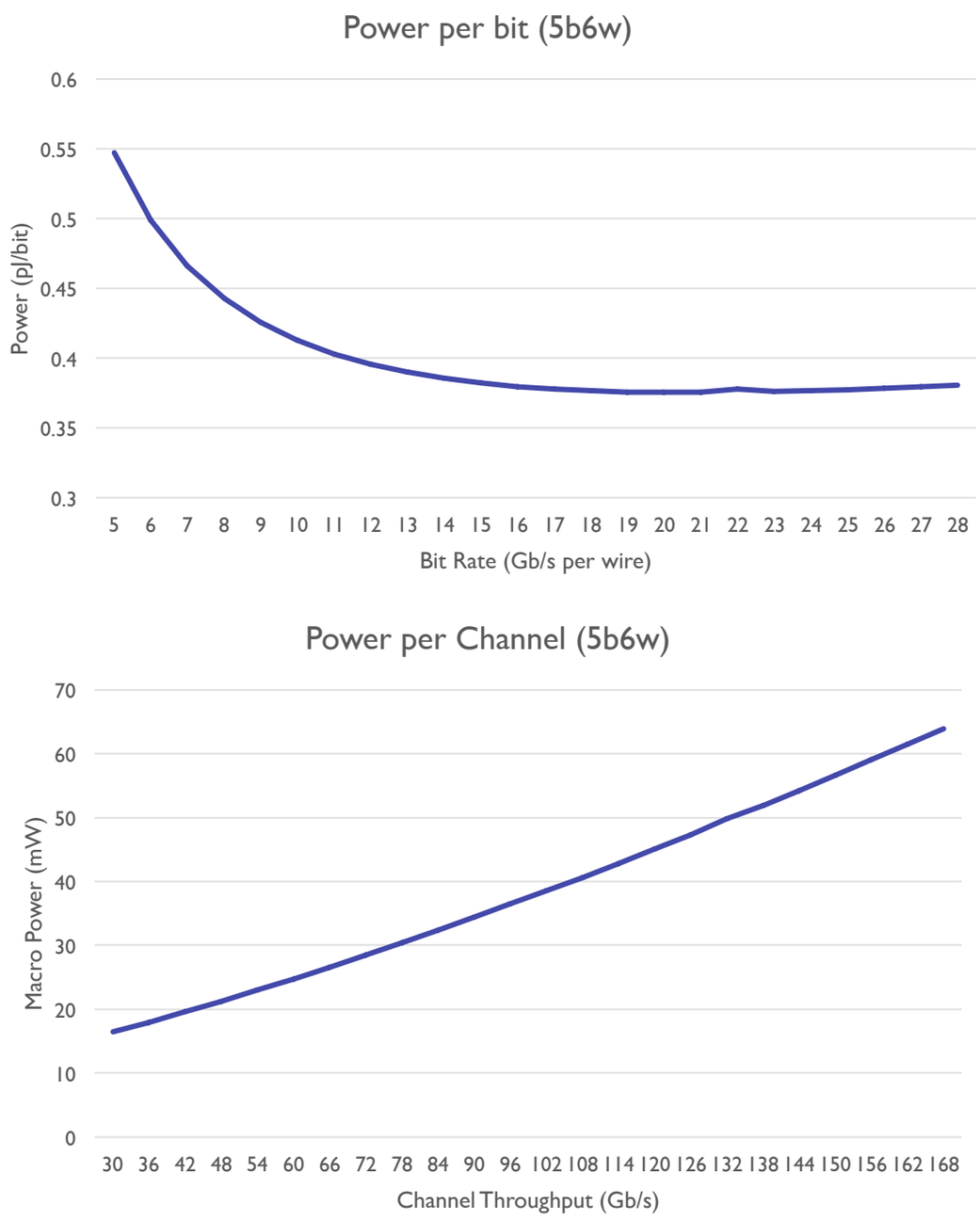
- Typical Power is 0.38 pJ/bit @19.2 Gbd.
- Power estimate based on:
  - Single Glasswing 5b/6w channel (full duplex)
  - Clock Tx/Rx shared and amortized over 2 channels.
  - 19.2 Gbaud/s (= 16 Gb/s per wire or 96 Gb/s per channel)
  - 16 nm process
- Architecture features to minimize power for extra short reach applications:
  - Clock forwarding (eliminates CDRs)
  - Reduced Tx amplitude (200 mVppd)
  - Reference clock supplied by chip level PLL (shared by all interfaces – not included in power estimate).



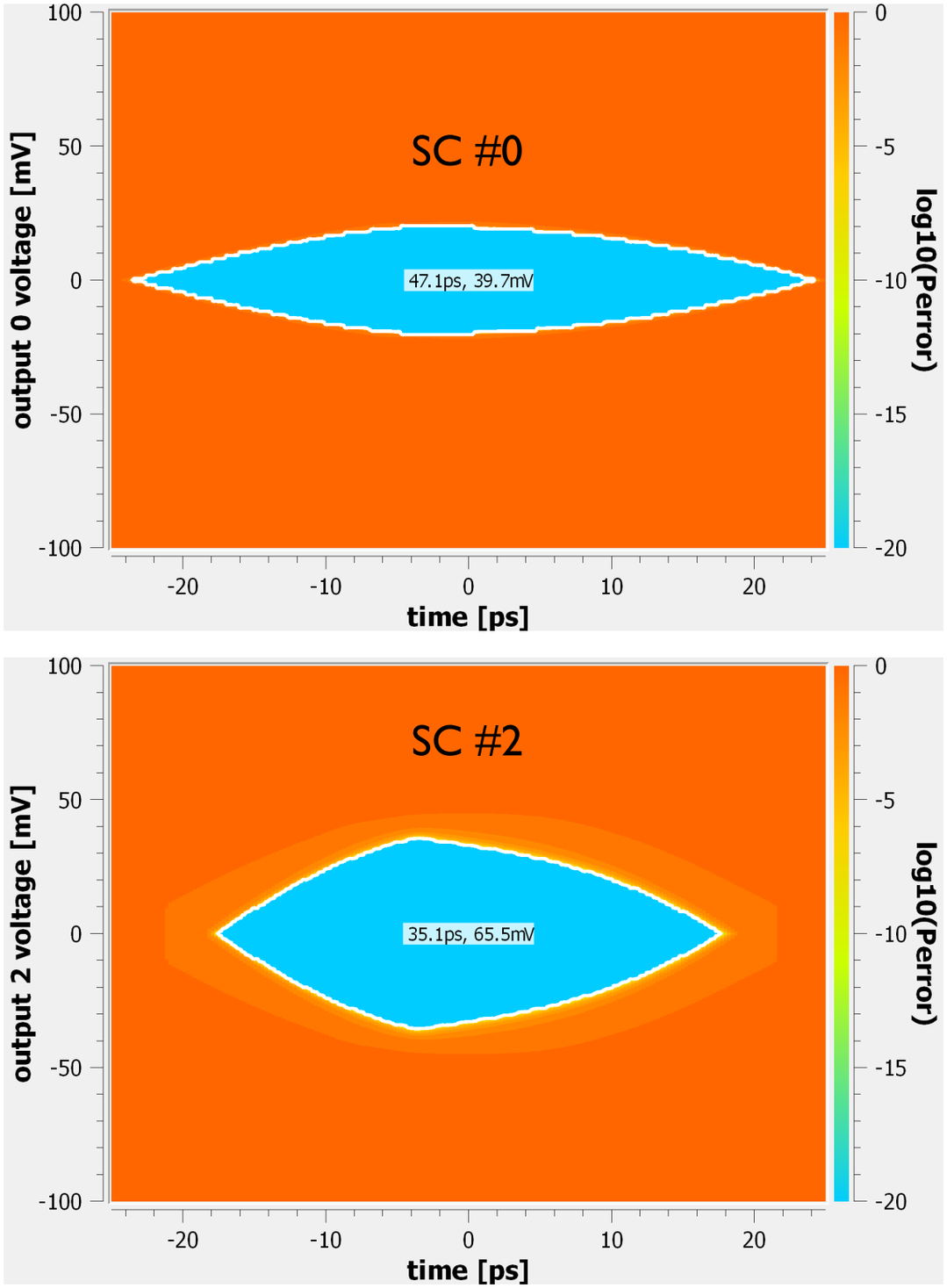
Power Total (mW)		35.21
Data Throughput (Gb/s)		96.00
Energy per Bit (pJ/bit)		0.38

Power vs. Baud Rate

- Primary power contributors are:
  - Output drivers / mux
  - Input sense amps
  - Clock trees
  - Termination Power
- Above ~15 Gb/s/wire, power scales approx. with frequency
  - ~0.38 pJ/bit up to range of 28 Gb/s/wire
  - ~0.55 pJ/bit at lower baud rates
- 28 Gb/s/wire is equivalent throughput to 56 Gb/s differential NRZ.



Signal Integrity Simulations



- Simulation conditions:
  - 20 Gbd/s
  - 5 cm strip-line routed as 3 diff. pairs
  - 100 fF ESD capacitance
- Sub-channel eyes:
  - ≥ 0.70 UI (35.10 ps) (limited by sc#2)
  - ≥ 39.65 mVppd (limited by sc#0)

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