10.1 A Pin-Efficient 20.83Gb/s/wire 0.94pJ/bit Forwarded Clock CNRZ-5-Coded SerDes up to 12mm for MCM Packages in 28nm CMOS

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High-speed signaling over package substrates is key to delivering the promise of 2.5D integration. Applications abound and include high-density memory interfaces, sub-division of large dies to increase yield and lower development time, sub-division of a die to achieve upward or downward scalability, or connecting to an off-chip SerDes or optics engine. Each of these in-package applications typically has high throughput and enormously low power constraints along with a low-loss channel. Several solutions have been proposed. Interposer substrates [1], or Chip-on-Substrate-on-Wafer [2] allow for very high-density wiring and low power using CMOS transceivers. Their high manufacturing and testing cost makes them prohibitive for anything but high-end applications. A different approach using high-speed ground-referenced single-ended signaling is reported in [3], which is intended for shorter channels up to 4.5mm and a BER of 1e-12. An approach using differential signaling on up to 0.75" of Megtron 6 material and a BER of 1e-9 is reported in [4]. A comparison is given in Fig. 10.1.1.

Our approach generalizes differential signaling. Correlated quaternary values are transmitted on a 6-wire bus with a forwarded clock (FCLK) SerDes, which achieves high bandwidth, coupled with low power. The set of transmitted values belongs to a code consisting of 32 codewords called the CNRZ-5-code. 5b are transmitted on the 6 wires in every UI. The codebook consists of judiciously chosen permutations of [+1, +1/3, +1/3, -1/3, -1/3, -1]. At the receiver, the codewords are detected by the 5 self-referencing comparators shown in Fig. 10.1.2. The specific choice of the codewords eliminates transmit common-mode and simultaneous switching output noise. The CNRZ-5 codebook and its comparators have been designed to optimize the ISI-Ratio [5], a figure of merit that measures the susceptibility of a signaling code to inter-symbol Interference (ISI). The smallest possible ISI-ratio is 1 and is achieved by both the differential NRZ and the 6-wire CNRZ-5 codes by design. Traditional quaternary signaling codes like differential PAM-4 have an ISI-ratio of 3, making them inherently much more susceptible to inter-symbol Interference (ISI). The susceptibility of a signaling code to inter-symbol Interference (ISI) is determined by the ratio of the signal power to the noise power in the vicinity of a symbol transition. The CNRZ-5 codebook is designed to minimize this ratio by carefully selecting the codewords so that the energy of a symbol transition is spread over a wider bandwidth than in other signaling schemes.

The CNRZ-5 SerDes in 28nm CMOS comprises a transmitter, Tx, a receiver, Rx, and a common block, CB. The transmitter consists of 6 data and 2 clock wires dedicated to the FCLK CDA, which is sampling data crossings. The self-referencing comparators provide immunity to common-mode noise across the 6 input data wires. T-coils (layers M8–M9) are used to compensate the parasitic input capacitance and achieve the desired input return loss. They are placed under the bumps to save area. The samplers have wide-range 7b low-speed offset-correction DACs with a resolution of 2.5mV. They can be used to reconstruct a receive eye at the output of the CTLE. The 6 Rx data wires and receive signal path circuitry are closely sketched up. A local Rx mini-PLL generates a local quarter-rate clock from the received FCLK; the Rx mini-PLL generates four clock phases (0, 90, 180, 270) using a complementary 4-stage forward Ring Oscillator (RO), which also provides an additional 315 degree phase for the CDA algorithm. The Rx mini-PLL maximizes bandwidth, and minimizes jitter transfer peaking.

A central low phase noise RO-based main-PLL generates a 3.125GHz clock from common RefClk frequencies. The main-PLL is a three-stage pseudo-differential RO supplied by a regulator from a 1.5V/1.8V supply. It has a programmable power efficiency of 0.94pJ/bit at 25Gb/s. The main-PLL provides the Tx clocks.

The CNRZ-5 FCLK SerDes link is fabricated in a 28nm 1P9M process. Its layout is shown in Fig. 10.1.5 and the testchip, with a single instance of the SerDes, is shown in Fig. 10.1.7. The SerDes size is 1.503±0.4185mm² (Si) and has been laid out in a modular fashion such that additional 6 wire channels may be added to the testchip. The testchip achieves 166Gb/s per mm die-edge (Rx plus Tx). A quad chord SerDes will offer 444Gb/s per mm (Rx plus Tx) with standard 150µm pitch bump technology. The FCLK SerDes supports data rates from 12.5 to 25Gbaud, internal Tx to Rx loop-back, PRBS31 and user pattern generation and verification, and a receiver eye. The test setup is a MCM with four testchips designed to support 3 MCM channels of lengths 5mm, 12mm and 24mm; two of the four die provide Tx and Rx 8-wire breakouts respectively. Figure 10.1.6 shows a horizontal bathtub plot with an opening of 20ps at BER=1E-15, and an example of an eye diagram using the on-die eyeoscope at 25Gbaud over 12mm of MCM trace with 1.3b loss; residual untracked jitter is 500fs (0.015UI). Long runs show a vertical eye opening of 6.6UI at 25Gb/s (V_{1/2}=49mV) at a nominal data rate of 166Gb/s (V_{1/2}=49mV) at 1.5V per PMOS-FET to track the jitter on the received signal, the Rx mini-PLL has a higher bandwidth (500MHz). The main-PLL is part of the common-block layout that also provides an analog test bus and temperature sensors. The Rx and Tx mini-PLLs are part of the Rx and Tx blocks, respectively, and include lock detectors.

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References:
Table 10.1.1: Comparison to prior work (SiCa=Silicon carrier, SE = single ended, D = differential, GRSE=ground referenced single-ended, MCM = MCM organic substrate, Meg 6 = Megtron 6) and power/area breakdown.

<table>
<thead>
<tr>
<th>Reference</th>
<th>[1]</th>
<th>[2]</th>
<th>[3]</th>
<th>[4]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>pW/tb</td>
<td>1.9</td>
<td>0.34</td>
<td>1.4</td>
<td>0.96</td>
<td>0.56</td>
</tr>
<tr>
<td>BW (GHz)</td>
<td>8.9</td>
<td>1.1</td>
<td>20</td>
<td>6</td>
<td>20.83</td>
</tr>
<tr>
<td>Technology</td>
<td>45 nm</td>
<td>45 nm</td>
<td>32 nm</td>
<td>32 nm</td>
<td>28 nm</td>
</tr>
<tr>
<td>Channel loss</td>
<td>≤ 20 dB</td>
<td>NA</td>
<td>≤ 1 dB</td>
<td>≤ 3 dB</td>
<td>≤ 3 dB</td>
</tr>
<tr>
<td>Substrate</td>
<td>SiCa</td>
<td>SiCa</td>
<td>MCM</td>
<td>MCM</td>
<td>MCM</td>
</tr>
<tr>
<td>Reach (mm)</td>
<td>≤ 40</td>
<td>≤ 11</td>
<td>≤ 4.5</td>
<td>≤ 16</td>
<td>≤ 12</td>
</tr>
<tr>
<td>BER</td>
<td>1e-9</td>
<td>5e-12</td>
<td>1e-9</td>
<td>1e-10</td>
<td>1e-15</td>
</tr>
</tbody>
</table>

Figure 10.1.1: Comparison to prior work (SiCa=Silicon carrier, SE = single ended, D = differential, GRSE=ground referenced single-ended, MCM = MCM organic substrate, Meg 6 = Megtron 6) and power/area breakdown.

Figure 10.1.2: Functional diagram of the CNRZ-5: encoder, wires, multi-input comparators.

Figure 10.1.3: CNRZ-5 transmitter block/circuit diagram.

Figure 10.1.4: CNRZ-5 receiver block/circuit diagram.

Figure 10.1.5: CNRZ-5 IP layout (CmIP = Common IP).

Figure 10.1.6: CNRZ-5 horizontal BER bathtub curve and example eye plot at the Rx for a 12mm MCM channel at 25Gb/s, PRBS31 pattern.
Figure 10.1.7: CNRZ-5 testchip.